

Author Index for Papers in Volume 24

Pages are numbered consecutively through the volume: 1-104, January; 105-264, March; 265-424, May; 425-528, July; 529-656, September; and 657-800, November. Communications are identified by (C).

Adams, G. G.

512 *Procedures for the Study of the Flexible-Disk to Head Interface*

Ahuja, Vijay

49 *Determining Deadlock Exposure for a Class of Store and Forward Communication Networks*

Allen, F. E., J. L. Carter, J. Fabri, J. Ferrante, W. H. Harrison, P. G. Loewner, and L. H. Trevillyan

695 *The Experimental Compiling System*

Ames, I.

188 *An Overview of Materials and Process Aspects of Josephson Integrated Circuit Fabrication*

Ames, I.

195 see Greiner, J. H.

Anacker, W.

107 *Josephson Computer Technology: An IBM Research Project*

Av-Ron, Moshe

469 see Shatzkes, Morris

Baker, John M.

195 see Greiner, J. H.

Baker, John M., C. J. Kircher, and J. W. Matthews

223 *Structure of Tunnel Barrier Oxide for Pb-Alloy Josephson Junctions*

Bar-Gadda, O.

328 see Tzou, A.

Bard, Yonathan

563 *Estimation of State Probabilities Using the Maximum Entropy Principle*

Basavaiah, S.

195 see Greiner, J. H.

Becerril, J. L., J. Bondia, R. Casajuana, and F. Valer

756 *Grammar Characterization of Flowgraphs*

Beeteson, J. S., K. T. Jarzebowski, and B. R. Sowter

598 *Digital System for Convergence of Three-Beam High-Resolution Color Data Displays*

Bhattacharyya, A., D. P. Gaffney, R. A. Kenyon, P. B. Mollier, J. E. Selleck, and F. W. Wiedman

378 *I/N Circuit and Device Technology*

Blaser, E.

328 see Tzou, A.

Bondia, J.

756 see Becerril, J. L.

Bossen, D. C. and M. Y. Hsiao

390 *A System Solution to the Memory Soft Error Problem*

Boyle, D., P. Mundy, and T. M. Spence

677 *Optimization and Code Generation in a Compiler for Several Machines*

Braunecker, B. U.

89 *Pattern Optimization for UPC Supermarket Scanner*

Broom, R. F., R. Jaggi, Th. O. Mohr, and A. Oosenbrug

206 *Effect of Process Variables on Electrical Properties of Pb-Alloy Josephson Junctions*

Broom, R. F., W. Kotyczka, and A. Moser

178 *Modeling of Characteristics for Josephson Junctions Having Nonuniform Width or Josephson Current Density*

Broom, R. F., R. B. Laibowitz, Th. O. Mohr, and W. Walter

212 *Fabrication and Properties of Niobium Josephson Tunnel Junctions*

Brosious, P. R.

195 see Greiner, J. H.

Brown, Alan V.

167 *An Overview of Josephson Packaging*

Canavello, B. J.

452 see Hatzakis, M.

Carballo, R.

328 see Tzou, A.

Carter, J. L.

695 see Allen, F. E.

Casajuana, R.

756 see Becerril, J. L.

Chai, Hi Dong

622 see Lee, Ho Chong

Chang, T. H. P.

537 see Grobman, W. D.

Chung, K. M., F. Luccio, and C. K. Wong

75 *On the Complexity of Permuting Records in Magnetic Bubble Memory Systems*

Cocke, John and Peter W. Markstein

692 *Strength Reduction for Division and Modulo with Application to Accessing a Multilevel Store (C)*

Cramer, Alice

339 see Rideout, V. Leo

Curtis, Huntington W.

370 see Verkuil, Roger L.

Davis, Donald E.

545 *Registration Mark Detection for Electron-Beam Lithography—ELI System*

Denil, N. J.

732 *A Business Language*

Donath, W. E.

480 *Stand-Alone Wiring Program for Josephson Logic*

Dreckmann, M.

398 see Stapper, C. H.

Eichelberger, E. B. and E. Lindbloom

15 *A Heuristic Test-Pattern Generator for Programmable Logic Arrays*

Fabri, J.

695 see Allen, F. E.

Faris, S. M., W. H. Henkels, E. A. Valsamakis, and H. H. Zappe

143 *Basic Design of a Josephson Technology Cache Memory*

Ferrante, J.

695 see Allen, F. E.

Fitzgerald, B. F. and E. P. Thoma

291 *Circuit Implementation of Fusible Redundant Addresses on RAMs for Productivity Enhancement*

Franaszek, Peter A.

638 *A General Method for Channel Coding (C)*

- Franaszek, P. A.**
43 *Synchronous Bounded Delay Coding for Input Restricted Channels*
- Gaffney, D. P.**
378 see Bhattacharyya, A.
- Gaind, A. K.**
348 see Kasprzak, L. A.
- Gardiner, J. R.**
353 see Ormond, D. W.
- Gdula, Robert A.**
469 see Shatzkes, Morris
- Geipel, H. J. and R. B. Shasteen**
362 *Implanted Source/Drain Junctions for Polysilicon Gate Technologies*
- Geipel, H. J. and W. K. Tice**
310 *Reduction of Leakage by Implantation Gettering in VLSI Circuits*
- Gheewala, T. R.**
130 *Design of 2.5-Micrometer Josephson Current Injection Logic (CIL)*
- Golden, R. L., P. A. Latus, and P. Lowy**
23 *Design Automation and the Programmable Logic Array Macro*
- Gopalakrishna, Y.**
328 see Tzou, A.
- Gray, Kenneth S.**
283 *Cross-Coupled Charge-Transfer Sense Amplifier and Latch Sense Scheme for High-Density FET Memories*
- Greenhaus, H.**
410 see Ho, I. T.
- Greiner, J. H., C. J. Kircher, S. P. Klepner, S. K. Lahiri, A. J. Warnecke, S. Basavaiah, E. T. Yen, John M. Baker, P. R. Brosious, H.-C. W. Huang, M. Murakami, and I. Ames**
195 *Fabrication Process for Josephson Integrated Circuits*
- Grobman, W. D., A. J. Speth, and T. H. P. Chang**
537 *Proximity Correction Enhancements for 1- μ m Dense Circuits*
- Grossman, D. D.**
64 see Wesley, M. A.
- Gu  ret, P., A. Moser, and P. Wolf**
155 *Investigations for a Josephson Computer Main Memory with Single-Flux-Quantum Cells*
- H  nsch, T. W.**
85 see Pole, R. V.
- Harrison, W. H.**
695 see Allen, F. E.
- Hatzakis, M., B. J. Canavello, and J. M. Shaw**
452 *Single-Step Optical Lift-Off Process*
- Heidelberger, Philip**
570 *Variance Reduction Techniques for the Simulation of Markov Processes, I: Multiple Estimates*
- Henkels, W. H.**
143 see Faris, S. M.
- Herrell, D. J.**
172 see Jones, H. C.
- Ho, I. T., J. Riseman, and H. Greenhaus**
410 *A Charge Injection Transistor Memory Cell (C)*
- Hsiao, M. Y.**
390 see Bossen, D. C.
- Huang, H.-C. W.**
195 see Greiner, J. H.
- Jaggi, R.**
206 see Broom, R. F.
- Jarzebowski, K. T.**
598 see Beeteson, J. S.
- Jones, H. C. and D. J. Herrell**
172 *The Characteristics of Chip-to-Chip Signal Propagation in a Package Suitable for Superconducting Circuits*
- Kasami, Tadao**
486 see Lin, Shu
- Kasprzak, L. A. and A. K. Gaind**
348 *Near-Ideal Si-SiO₂ Interfaces*
- Kenyon, R. A.**
378 see Bhattacharyya, A.
- Kircher, C. J.**
223 see Baker, John M.
- Kircher, C. J.**
195 see Greiner, J. H.
- Kircher, C. J. and S. K. Lahiri**
235 *Properties of AuIn₂ Resistors for Josephson Integrated Circuits*
- Klepner, S. P.**
195 see Greiner, J. H.
- Kolsky, Harwood G.**
660 see Scarborough, Randolph G.
- Kotyczka, W.**
178 see Broom, R. F.
- Kyser, D. F. and R. Pyle**
426 *Computer Simulation of Electron-Beam Resist Profiles*
- Lafuente, J. M.**
716 *Some Techniques for Compile-Time Analysis of User-Computer Interactions*
- Lahiri, S. K.**
195 see Greiner, J. H.
- Lahiri, S. K.**
235 see Kircher, C. J.
- Laibowitz, R. B.**
212 see Broom, R. F.
- Larsen, Richard A.**
268 *A Silicon and Aluminum Dynamic Memory Technology*
- Latus, P. A.**
23 see Golden, R. L.
- Lavin, M. A.**
64 see Wesley, M. A.
- Lee, Ho Chong and Hi Dong Chai**
622 *Integral Point-Matching Method for Two-Dimensional Laplace Field Problems with Periodic Boundaries*
- Lew, John S.**
496 *Optimal Accelerometer Layouts for Data Recovery in Signature Verification*
- Lieberman, L. I.**
64 see Wesley, M. A.
- Lin, Shu, Tadao Kasami, and Saburo Yamamura**
486 *Existence of Good δ -Decodable Codes for the Two-User Multiple-Access Adder Channel*
- Lin, Shu and George Markowsky**
56 *On a Class of One-Step Majority-Logic Decodable Cyclic Codes*
- Lindbloom, E.**
15 see Eichelberger, E. B.
- Lo, T. C., R. E. Scheuerlein, and R. Tamlyn**
318 *A 64K FET Dynamic Random Access Memory: Design Considerations and Description*

- Loewner, P. G.**
695 see Allen, F. E.
- Lomet, David B.**
764 *A Data Definition Facility Based on A Value-Oriented Storage Model*
- Lowy, P.**
23 see Golden, R. L.
- Lozano-Pérez, T.**
64 see Wesley, M. A.
- Luccio, F.**
75 see Chung, K. M.
- MacNair, Edward A.**
747 see Sauer, Charles H.
- Magerlein, J. H. and D. J. Webb**
554 *Electron-Beam Resists for Lift-Off Processing with Potential Application to Josephson Integrated Circuits*
- Markowsky, George**
56 see Lin, Shu
- Markowsky, George and Michael A. Wesley**
582 *Fleshing Out Wire Frames*
- Marks, Brian**
684 *Compilation to Compact Code*
- Markstein, Peter W.**
692 see Cocke, John
- Matisoo, J.**
113 *Overview of Josephson Technology Logic and Memory*
- Matthews, J. W.**
223 see Baker, John M.
- McLaren, A. N.**
398 see Stapper, C. H.
- Mohr, Th. O.**
206 see Broom, R. F.
- Mohr, Th. O.**
212 see Broom, R. F.
- Mollier, P. B.**
378 see Bhattacharyya, A.
- Moser, A.**
178 see Broom, R. F.
- Moser, A.**
155 see Guéret, P.
- Mundy, P.**
677 see Boyle, D.
- Murakami, M.**
195 see Greiner, J. H.
- Oosenbrug, A.**
206 see Broom, R. F.
- Ormond, D. W. and J. R. Gardiner**
353 *Reliability of SiO₂ Gate Dielectric with Semi-Recessed Oxide Isolation*
- Pak, Mun S.**
370 see Verkuil, Roger L.
- Parikh, Mihir**
438 *Proximity Effects in Electron Lithography: Magnitude and Correction Techniques*
- Parikh, Mihir and Donald E. Schreiber**
530 *Pattern Partitioning for Enhanced Proximity-Effect Corrections in Electron-Beam Lithography*
- Patel, Arvind M.**
32 *Error Recovery Scheme for the IBM 3850 Mass Storage System*
- Petersen, Kurt E.**
631 *Silicon Torsional Scanning Mirror*
- Pole, R. V., A. J. Spiekerman, and T. W. Hänsch**
85 *Interferometric Wavelength Measurements through Post-Detection Signal Processing*
- Pyle, R.**
426 see Kyser, D. F.
- Rideout, V. Leo, John J. Walker, and Alice Cramer**
339 *A One-Device Memory Cell Using a Single Layer of Polysilicon and a Self-Registering Metal-to-Polysilicon Contact*
- Riseman, J.**
410 see Ho, I. T.
- Rottmann, H. R.**
461 *Overlay in Lithography*
- Salza, Silvio**
747 see Sauer, Charles H.
- Sauer, Charles H., Edward A. MacNair, and Silvio Salza**
747 *A Language for Extended Queuing Network Models*
- Scarborough, Randolph G. and Harwood G. Kolsky**
660 *Improved Optimization of FORTRAN Object Programs*
- Scheuerlein, R. E.**
318 see Lo, T. C.
- Schmookler, Martin S.**
2 *Design of Large ALUs Using Multiple PLA Macros*
- Schreiber, Donald E.**
530 see Parikh, Mihir
- Selleck, J. E.**
378 see Bhattacharyya, A.
- Shasteen, R. B.**
362 see Geipel, H. J.
- Shatzkes, Morris, Moshe Av-Ron, and Robert A. Gdula**
469 *Defect-Related Breakdown and Conduction in SiO₂*
- Shaw, J. M.**
452 see Hatzakis, M.
- Sowter, B. R.**
598 see Beeteson, J. S.
- Spence, T. M.**
677 see Boyle, D.
- Speth, A. J.**
537 see Grobman, W. D.
- Spiekerman, A. J.**
85 see Pole, R. V.
- Stapper, C. H., A. N. McLaren, and M. Dreckmann**
398 *Yield Model for Productivity Optimization of VLSI Memory Chips with Redundancy and Partially Good Product*
- Tamlyn, R.**
318 see Lo, T. C.
- Thoma, E. P.**
291 see Fitzgerald, B. F.
- Tice, W. K.**
310 see Geipel, H. J.
- Trevillyan, L. H.**
695 see Allen, F. E.
- Troutman, R. R.**
299 *VLSI Device Phenomena in Dynamic Memory and Their Application to Technology Development and Device Design*
- Tsui, Frank F.**
243 *JSP—A Research Signal Processor in Josephson Technology*

Tzou, A., Y. Gopalakrishna, E. Blaser, O. Bar-Gadda, and R. Carballo

328 *A 256K-Bit Charge-Coupled Device Memory*

Valer, F.

756 see Becerril, J. L.

Valsamakis, E. A.

143 see Faris, S. M.

Vergnieres, Bernard

612 *Macro Generation Algorithms for LSI Custom Chip Design*

Verkuil, Roger L., Huntington W. Curtis, and Mun S. Pak

370 *A Contactless Method for High-Sensitivity Measurement of p-n Junction Leakage*

Walker, John J.

339 see Rideout, V. Leo

Walter, W.

212 see Broom, R. F.

Warnecke, A. J.

195 see Greiner, J. H.

Webb, D. J.

554 see Magerlein, J. H.

Wesley, Michael A.

582 see Markowsky, George

Wesley, M. A., T. Lozano-Pérez, L. I. Lieberman, M. A. Lavin, and D. D. Grossman

64 *A Geometric Modeling System for Automated Mechanical Assembly*

Wiedman, F. W.

378 see Bhattacharyya, A.

Wolf, P.

155 see Guéret, P.

Wong, C. K.

75 see Chung, K. M.

Yamamura, Saburo

486 see Lin, Shu

Yen, E. T.

195 see Greiner, J. H.

Zappe, H. H.

143 see Faris, S. M.